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Creating an AXI Peripheral in Vivado Learn how to create an **AXI** peripheral to which custom logic can be added to create a custom IP using the Create and Package IP ...

ZYNQ Training - Session 01 - What is AXI? Web Page for this lesson : http://www.googoolia.com/wp/2014/03/20/lesson-1-what-is-**axi**-part-1/ This video gives a very basic ...

Creating a custom AXI-Streaming IP in Vivado How to create a custom AXI-Streaming IP in Vivado and test it with AXI DMA on the MicroZed 7010

ZYNQ Training - Session 04 - Designing with AXI using Xilinx Vivado Web page for this lesson: http://www.googoolia.com/wp/2014/04/15/lesson-4-designing...**axi**-using-**xilinx**-**vivado**/ This video is ...

PCIe Development with FPGA: Section 5 Lab51 loading ILA data and analyzing the PCIe Packets Udemy Course Coupon Link: https://www.udemy.com/pci-express-development-with-fpga/?... ...

Specifying AXI4 Lite Interfaces for your Vivado System Generator Design Final Learn how System Generator provides AXI4-Lite abstraction making it possible to incorporate a DSP design into an embedded ...

MATLAB as AXI Master with Xilinx FPGA and Zynq SoC Boards Performing interactive testing on FPGA boards is a popular way to verify designs and perform parametric testing. See how HDL ...

ZYNQ Training - session 03 - axi stream interface Web page for this lesson: http://www.googoolia.com/wp/2014/04/12/lesson-3-**axi**-stream-interface/ What is an **AXI** stream Interface ...

Video Streaming with ZedBoard: AES FMC HDMI CAM Interfacing with HDMI in and HDMI out This Tutorial is on How to interface Avnet FMC-HDMI-CAM Module and ZedBoard FPGA. Please write to info@logictronix.com or ...

DMA for PCI Express This video walks through the process of creating a PCI Express solution that uses the new 2016.1 DMA for PCI Express IP ...

Zybo Zynq-7000 DMA Audio Project Demo The ZYBO board I use in this video has been discontinued. Here is a link to a comparison between the board I used (ZYBO) and ...

VIVADO HLS Training - AXI Lite slave floating point #5 Hi guys today we're going to learn how to create axi4-Lite slave interfaces on your generated ip core, to illistrate this process ...

Using Vivado with Xilinx Evaluation Boards Learn how the board-aware features of the **Vivado** Design suite can be used to quickly configure and implement designs targeting ...

ZYNQ Training - session 07 part I - AXI Stream Interfaces in Detail (RTL Flow) Web page for this lesson: http://www.googoolia.com/wp/2014/05/31/lesson-7-**axi**-stream-interface-in-detail-rtl-flow/ In this video ...

Implementing AXI in Verilog Part 1: Slave Interface In this video I describe the interface to a Verilog module for an **AXI** slave that controls access to a RAM.

What is AXI Lite? In this video I explain the AXI4 lite bus protocol by building it up from a simple RAM interface.

Creating Custom AXI Slave Interfaces Part 1 (Lesson 6) Sourcecode available here: http://ems.eit.uni-kl.de/index.php?id=367 The **Xilinx** ZYNQ Training Video-**Book**, will contain a series ...

Xilinx Zynq UltraScale RFSoCs multi-gigasample RF data converters and SD-FEC **Xilinx** is the inventor of the FPGA, hardware programmable SoCs, and now, the ACAP. Zynq UltraScale RFSoCs integrate ...

Custom IP Upload to Zedboard Revision D in QSPI JTAG Mode via Xilinx VIVADO SDK For more insights on Creating Custom IP and Embedded System $9.99 Udemy Course Coupon of Embedded System Design with ...

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